

# voltage\_divider\_routed

Design Report

Rev 1 | 2026-09-10 | jlcpcb

kicad-tools 0.20.0

## Board Summary

| Property   | Value                     |
|------------|---------------------------|
| Layers     | 2 copper (F.Cu, B.Cu)     |
| Footprints | 4 (2 SMD, 2 THT, 0 other) |
| Nets       | 3                         |
| Traces     | 21 segments               |
| Vias       | 2                         |
| Board Size | 30.0 x 25.0 mm            |

## Design Overview

### Theory of Operation

Voltage Divider Test

Simple 2-resistor voltage divider

5V -> 2.5V (10k/10k)

## Power Architecture

**Power Rails:** GND, PWR\_FLAG

## Hand-Solder (THT) Components

---

The following 2 through-hole components are **excluded from the SMT pick-and-place file** and must be hand-soldered (or wave/selective-soldered) after SMT assembly. They appear in the BOM for sourcing.

| Value | Package                             | Qty | References |
|-------|-------------------------------------|-----|------------|
| IN    | PinHeader_1x02_P2.54<br>mm_Vertical | 1   | J1         |
| OUT   | PinHeader_1x02_P2.54<br>mm_Vertical | 1   | J2         |

## ERC Status

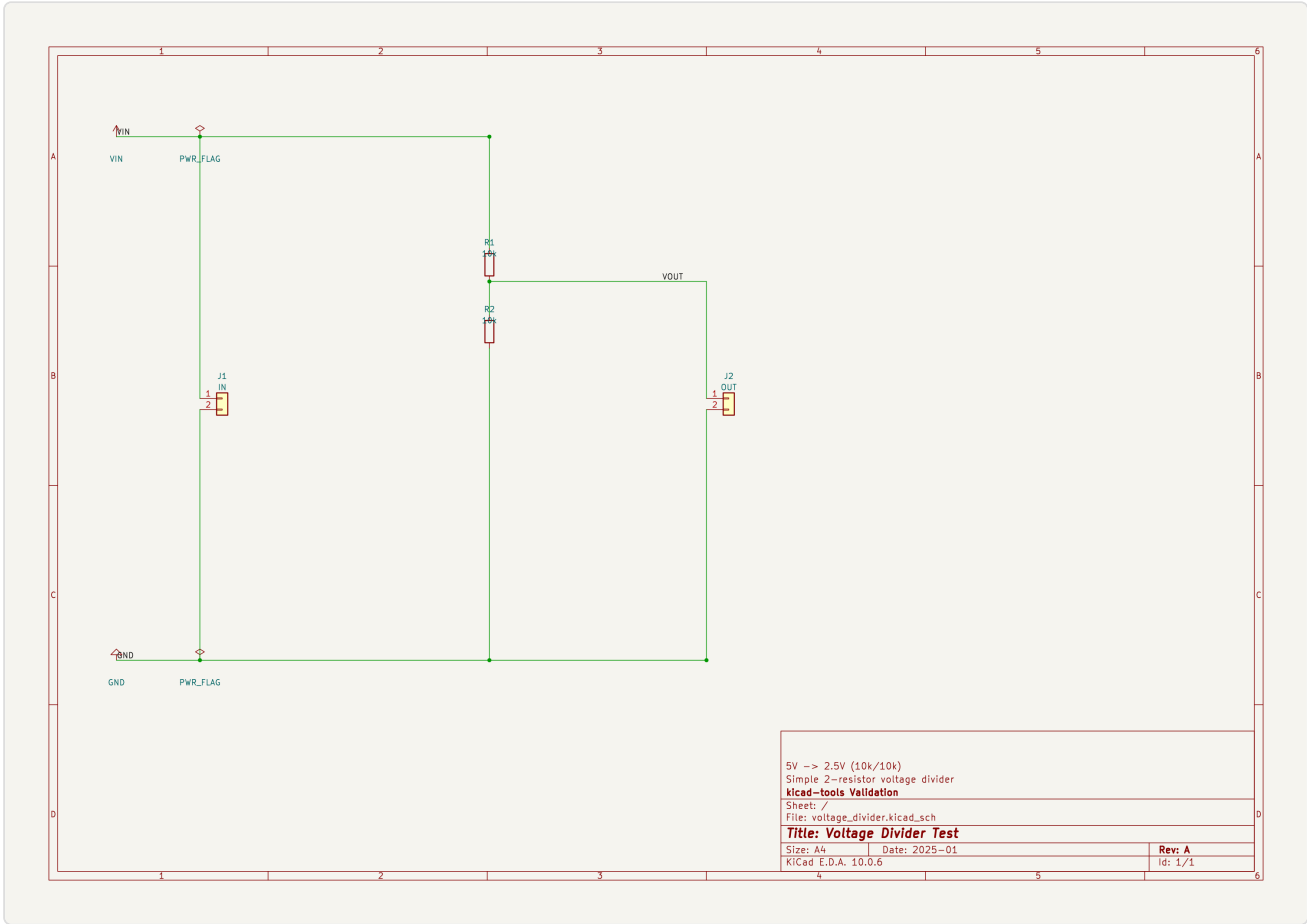
---

| Metric   | Count |
|----------|-------|
| Errors   | 0     |
| Warnings | 0     |

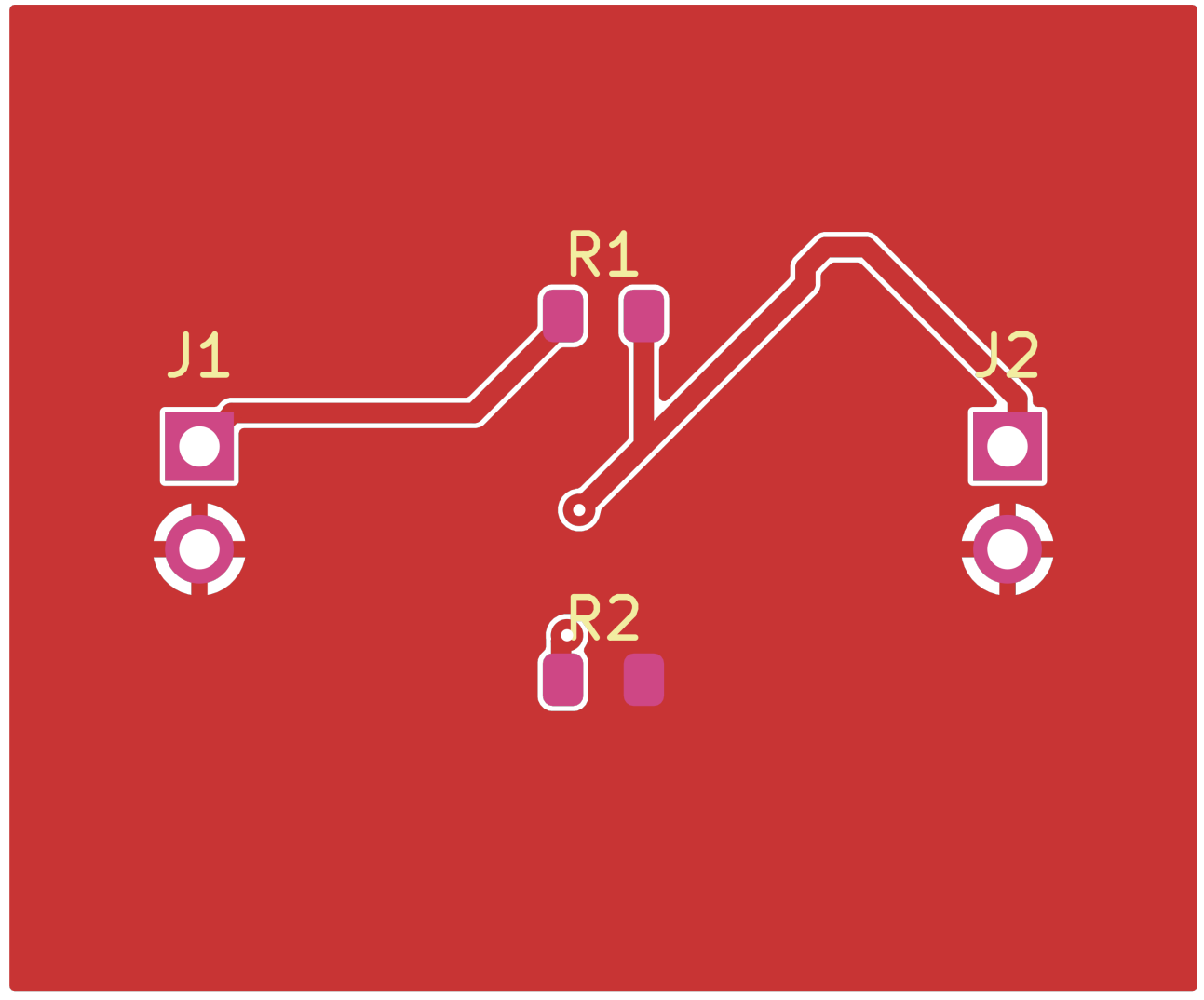
**Status:** SKIPPED -- ERC skipped by user request

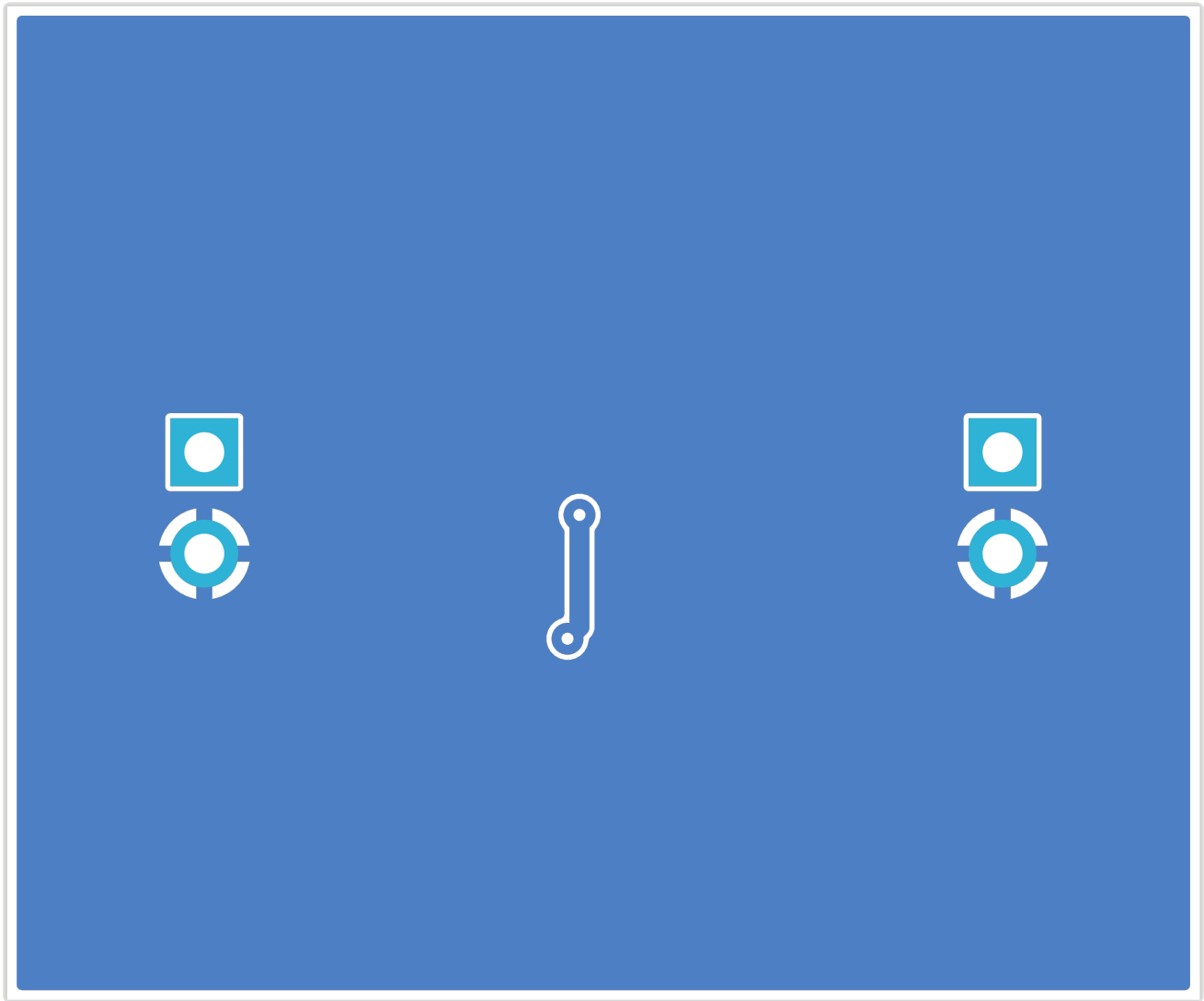
# Schematic Overview

## Schematic: voltage\_divider

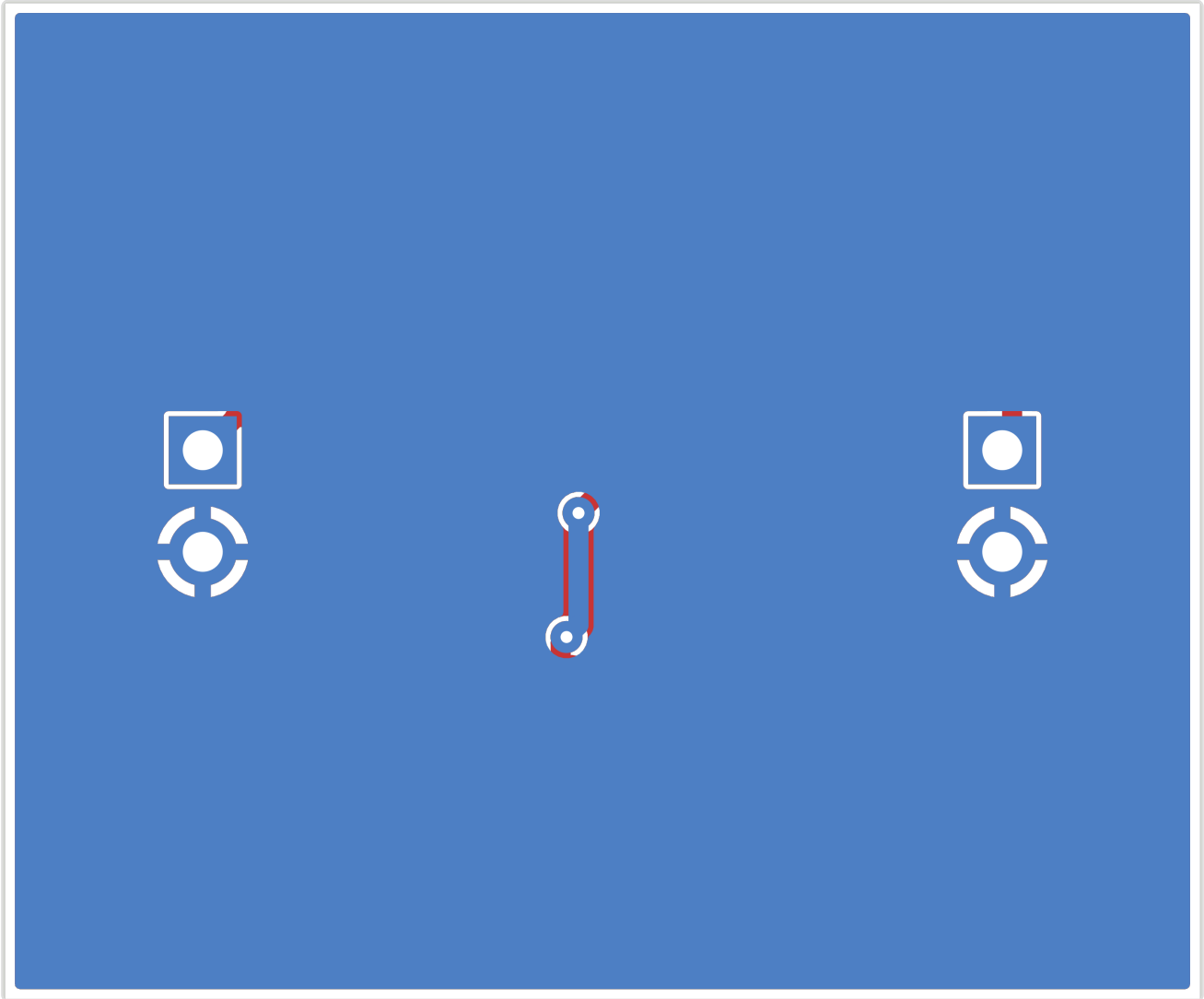


## PCB Layout

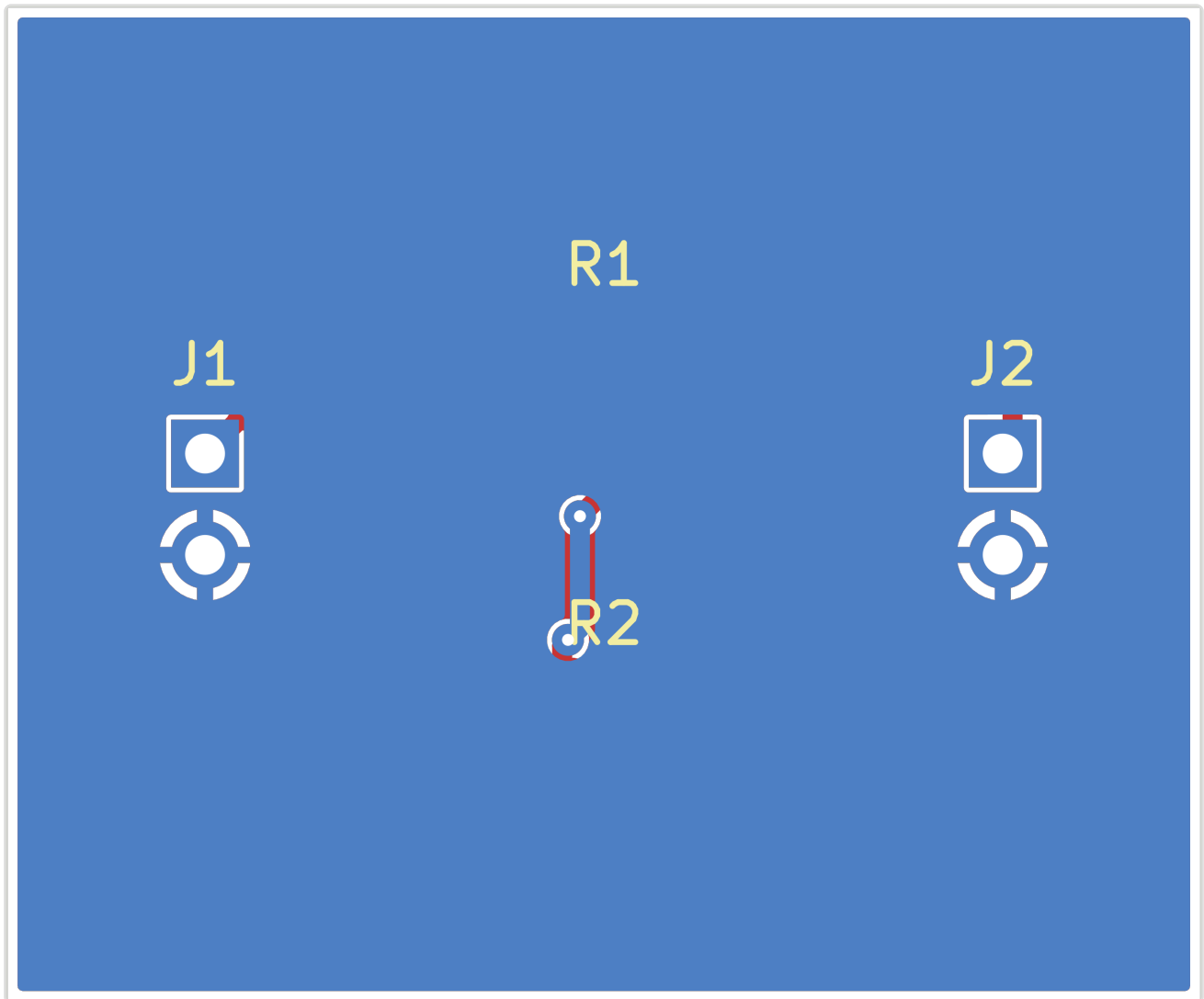




## Copper



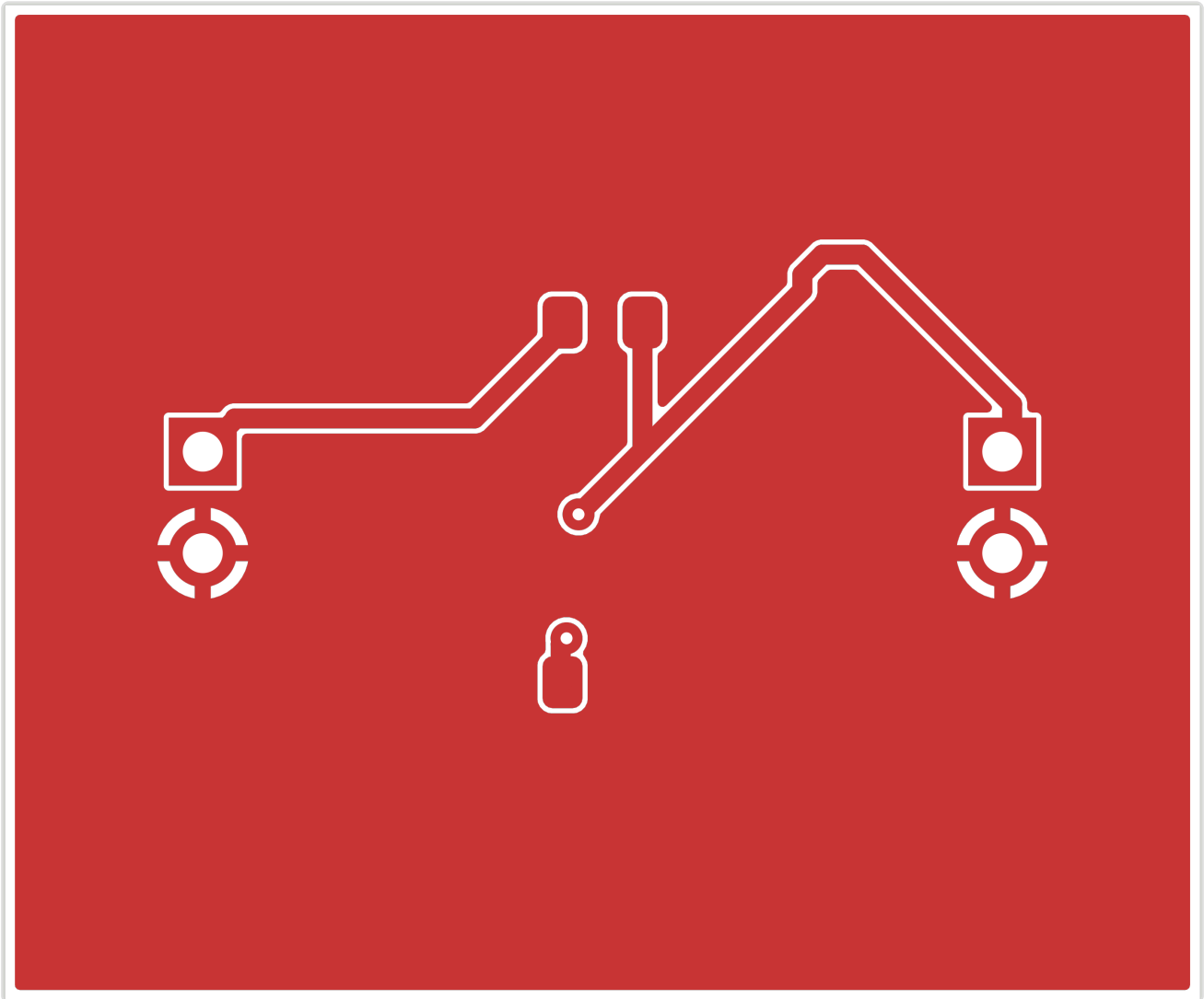
## Assembly



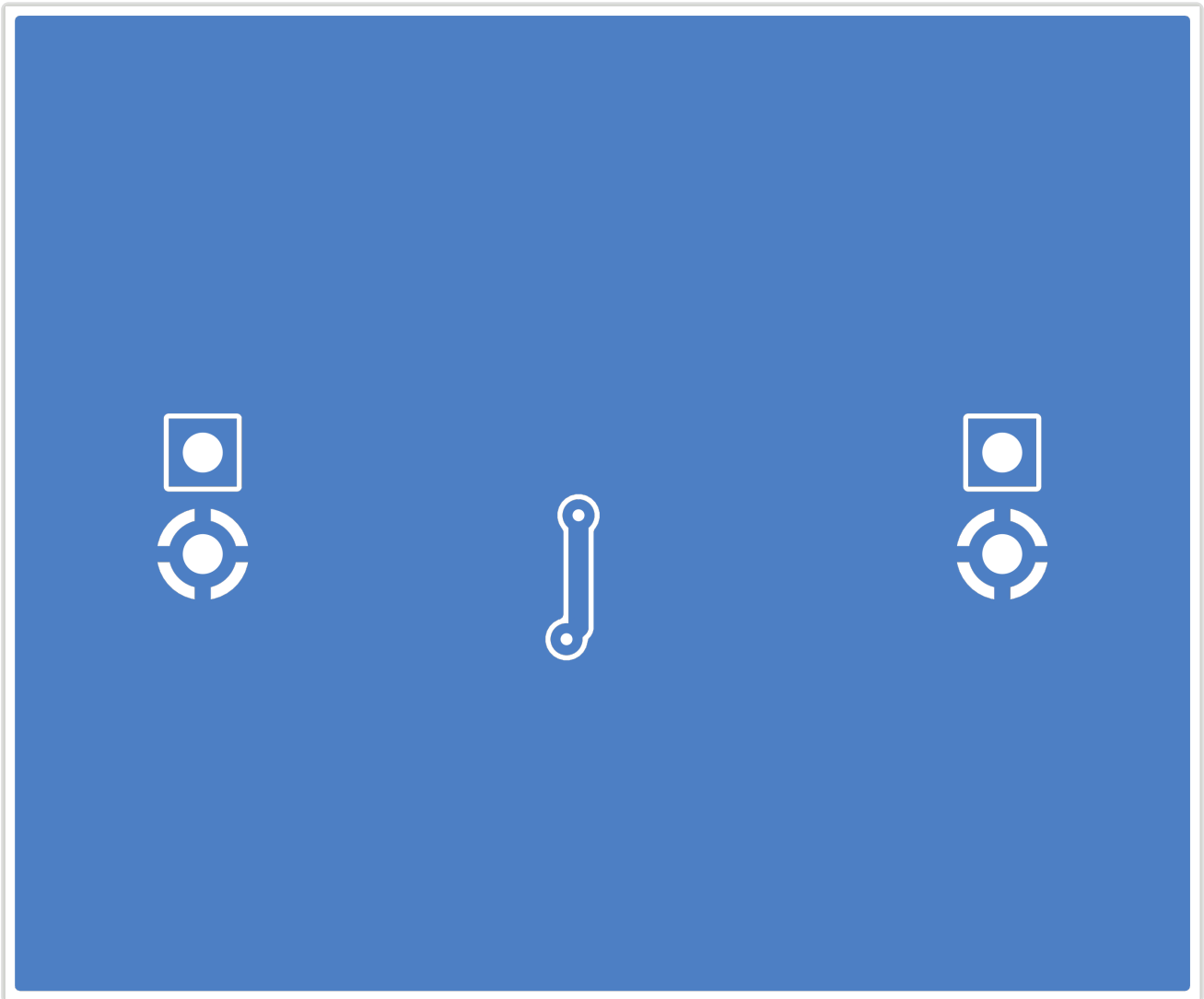
## Copper Layers

---

F.Cu



## B.Cu



## Bill of Materials

| Value | Package                             | Qty | References |
|-------|-------------------------------------|-----|------------|
| IN    | PinHeader_1x02_P2.54<br>mm_Vertical | 1   | J1         |
| OUT   | PinHeader_1x02_P2.54<br>mm_Vertical | 1   | J2         |
| 10k   | R_0805_2012Metric                   | 2   | R1, R2     |

# DRC Status

| Metric   | Count |
|----------|-------|
| Errors   | 0     |
| Warnings | 0     |
| Blocking | 0     |

Status: PASS

## Manufacturing Readiness

---

**Verdict:** READY

### Action Items

- **[OPTIONAL]** Verify zone fill in KiCad for 1 zone-connected nets

## Routing Status

| Metric                | Value        |
|-----------------------|--------------|
| Signal Net Completion | 100.0% (2/2) |
| Overall Completion    | 100.0%       |
| Complete Nets         | 3 / 3        |
| Zone-Connected Nets   | 1            |
| Incomplete Nets       | 0            |
| Unconnected Pads      | 0            |

## Zone-Connected Nets

- GND

## Cost Estimate

| Metric                   | Per Board (estimated) |
|--------------------------|-----------------------|
| PCB Fabrication          | ~0.55 USD             |
| Components (estimated)   | ~0.21 USD             |
| Assembly (estimated)     | ~1.93 USD             |
| <b>Total (estimated)</b> | <b>~2.69 USD</b>      |
| Batch Quantity           | 5                     |
| Batch Total (estimated)  | ~13.44 USD            |